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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,858	01/19/2004	Tzueng-Yau Lin	MTKP0044USA	1857
27765 7590 05/22/2007 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER SAUNDERS JR, JOSEPH	
			ART UNIT	PAPER NUMBER
			2615	
			NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/707,858	Applicant(s) LIN, TZUENG-YAU	
	Examiner Joseph Saunders	Art Unit 2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
- 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
- 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>1-19-04, 3-19-04</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This is the initial office action based on the application filed January 19, 2004.

Claims 1 – 20 are currently pending and considered below.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 5 and 10 recites the limitation "the decoder". There is insufficient antecedent basis for this limitation in the claim. The examiner will interpret the limitation "the decoder" as "a decoder" when interpreting the claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 3, 6 – 8, 11 – 13 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Van Steenbrugge (6,076,062), hereinafter Van Steenbrugge.

Claim 1: Van Steenbrugge discloses an audio processing circuit (Figure 6) for receiving a first stream complying with a first standard (MPEG) and generating a second stream complying with a second standard which is a digital interface standard (IEC958) (Column 2 Lines 2 – 7), the first stream includes a plurality of frames, each of the frames includes a plurality of fields (Figures 4A – D), the audio processing circuit comprises: a stream buffer for storing the frames of the first stream ("FIFO 28 is provided that by way of example accommodates 8 k Bytes as generally required for intermediate storage of MPEG data," Column 5 Lines 33 – 35); a stream recovering circuit electrically connected to the stream buffer for detecting at least one of the plurality of fields in the frames (TD1315, Figure 10), modifying at least one of the plurality of fields according to the first standard, and generating modified frames ("If in block 122 an Audio bitstream is detected, in block 1126 it is detected whether a Gap occurs. If "Gap", in block 120 a PAUSE data burst is sent," Column 8 Lines 10 – 12); a first buffer electrically connected to the stream recovering circuit for storing the modified frames; and a burst circuit electrically connected to the first buffer for partitioning the modified frames into a plurality of payload sections, adding a preamble to each of the payload sections, and forming the second stream (TD1315 packages the burst payloads as user data in IEC958 format frames including a burst_preamble and a payload and therefore since the signal is a "burst" of data the first buffer is included and electrically connected within the recovering circuit for storing the modified frames before transmission, Column 8 Lines 45 – 57).

Claim 2: Van Steenbrugge discloses the audio processing circuit of claim 1 wherein the second standard is S/PDIF standard (IEC958).

Claim 3: Van Steenbrugge discloses the audio processing circuit of claim 1 wherein the first stream is retrieved from an optical storage disk (DVD player).

Claim 6: Van Steenbrugge discloses an audio processing circuit (Figure 6) for receiving a first stream complying with a first standard (MPEG) and generating a second stream complying with a second standard which is a digital interface standard (IEC958) (Column 2 Lines 2 – 7), the first stream includes a plurality of frames, each of the frames includes a plurality of fields (Figures 4A – D), the plurality of fields include a sync word field (Pa, Pb sync words), the audio processing circuit comprises: a stream buffer for storing the frames of the first stream ("FIFO 28 is provided that by way of example accommodates 8 k Bytes as generally required for intermediate storage of MPEG data," Column 5 Lines 33 – 35); a stream recovering circuit electrically connected to the stream buffer for receiving expected positions of the sync words derived from the first stream (TD1315, Figure 10), locating actual positions of the sync word fields by detecting neighborhood positions substantially close to the expected positions (TD1315 uses timing information, from timing control block 96, based on the sync words Pa, Pb in order to maintain synchronization of the parsed frames necessary for positioning the PAUSE burst for transfer, Column 4 Lines 55 – 58 and Column 7 Lines 49 – 52), modifying the frames according to the actual positions of the sync word fields, and

generating modified frames ("If in block 122 an Audio bitstream is detected, in block 1126 it is detected whether a Gap occurs. If "Gap", in block 120 a PAUSE data burst is sent," Column 8 Lines 10 – 12); a first buffer electrically connected to the stream recovering circuit for storing the modified frames; a burst circuit electrically connected to the first buffer for partitioning the modified frames into a plurality of payload sections, adding a preamble to each of the payload sections, and forming the second stream (TD1315 packages the burst payloads as user data in IEC958 format frames including a busrt_preamble and a payload and therefore since the signal is a "burst" of data the first buffer is included and electrically connected within the recovering circuit for storing the modified frames before transmission, Column 8 Lines 45 – 57).

Claim 7: Van Steenbrugge discloses the audio processing circuit of claim 1 wherein the second standard is S/PDIF standard (IEC958).

Claim 8: Van Steenbrugge discloses the audio processing circuit of claim 1 wherein the first stream is retrieved from an optical storage disk (DVD player).

Claim 11: Van Steenbrugge discloses a method for transferring a first stream complying with a first standard (MPEG) into a second stream complying with a second standard which is a digital interface standard (IEC958), the first stream includes a plurality of frames, each of the frames includes a plurality of fields (Figures 4A – D), the method comprises the steps of: detecting at least one of the plurality of fields in the frames,

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modifying at least one of the plurality of fields according to the first standard, and generating modified frames ("If in block 122 an Audio bitstream is detected, in block 1126 it is detected whether a Gap occurs. If "Gap", in block 120 a PAUSE data burst is sent," Column 8 Lines 10 – 12); and partitioning the modified frames into a plurality of payload sections, adding a preamble to each of the payload sections, and forming the second stream (TD1315 packages the burst payloads as user data in IEC958 format frames including a busrt_preamble and a payload and therefore since the signal is a "burst" of data the first buffer is included and electrically connected within the recovering circuit for storing the modified frames before transmission, Column 8 Lines 45 – 57).

Claim 12: Van Steenbrugge discloses the method of claim 11 wherein the first stream is retrieved from an optical storage disk (DVD player).

Claim 13: Van Steenbrugge discloses the method of claim 11 wherein the second standard is S/PDIF standard (IEC958).

Claim 16: Van Steenbrugge discloses the method of claim 11 wherein the modifying step further comprises changing a field of one of the frames of the first stream (A "Gap" is changed to a "Pause data-burst", Block 130 of Figure 12).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 4, 9, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Steenbrugge in view of Fujishita (US 6,988,013 B1), hereinafter Fujishita.

Claim 4: Van Steenbrugge discloses the audio processing circuit of claim 1 further comprising: a decoding circuit (MC decoder) electrically connected to the stream buffer (FIFO 28) for decoding the frames retrieved from the stream buffer; a second buffer electrically connected to the decoding circuit for storing decoded frames generated by the decoding circuit (Intermediate buffer 58, Figure 7). Van Steenbrugge does not disclose a digital to analog converter electrically connected to the second buffer for converting the decoded frames received from the second buffer to analog signals however Fujishita discloses a DVD player with circuitry to decode an MPEG audio stream and output multi-channel audio. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a D/A converter as disclosed by Fujishita after the decoder to allow for output of the multi-channel decoded signal to be converted into an analog signal, amplified, and sent to the appropriate speaker to output sound (Fujishita, Column 4 Lines 8 – Column 5 Line 13).

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Claim 9: Van Steenbrugge discloses the audio processing circuit of claim 1 further comprising: a decoding circuit (MC decoder) electrically connected to the stream buffer (FIFO 28) for decoding the frames retrieved from the stream buffer; a second buffer electrically connected to the decoding circuit for storing decoded frames generated by the decoding circuit (Intermediate buffer 58, Figure 7). Van Steenbrugge *does not disclose* a digital to analog converter electrically connected to the second buffer for converting the decoded frames received from the second buffer to analog signals however Fujishita discloses a DVD player with circuitry to decode an MPEG audio stream and output multi-channel audio. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a D/A converter as disclosed by Fujishita after the decoder to allow for output of the multi-channel decoded signal to be converted into an analog signal, amplified, and sent to the appropriate speaker to output sound (Fujishita, Column 4 Lines 8 – Column 5 Line 13).

Claim 14: Van Steenbrugge discloses the method of claim 11 further comprising decoding the frames of the first stream. Van Steenbrugge *does not disclose* converting the decoded frames into analog signals however Fujishita discloses a DVD player with circuitry to decode an MPEG audio stream and output multi-channel audio. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a D/A converter as disclosed by Fujishita after the decoder to allow for output of the multi-channel decoded signal to be converted into an analog signal, amplified, and sent to the appropriate speaker to output sound (Fujishita, Column 4 Lines 8 – Column

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5 Line 13).

9. Claims 5, 10, 15, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Steenbrugge in view of Matsuura et al. (US 2002/0181600), hereinafter Matsuura.

Claim 5: Van Steenbrugge discloses the audio processing circuit of claim 1 but does not disclose wherein a decoding circuit and the stream recovering circuit are integrated into an audio processor of the audio processing circuit. Matsuura discloses a method for converting a data stream of a first format possibly containing an error in to a correct data stream of a second format. Matsuura shows a TS separator that decodes or parses the mpeg stream similar to block 90 of Van Steenbrugge and Matsuura further discloses an error detecting and correcting unit that repackages the signal similar to block 32 Van Steenbrugge. Matsuura further shows both of separator and the error detecting and correcting unit being integrated into an audio processor (Figure 5 of Matsuura and Figure 10 of Van Steenbrugge). It would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the blocks 90 and 98 of Van Steenbrugge since having the decoder and error detecting and correcting integrated into an audio processor as disclosed by Matsuura eliminates the possibility of an error being passed on to a unit, similar to block 90, responsible for repackaging the stream into a second format and as a result a more accurate stream is obtained (Matsuura, Paragraphs 131 and 132).

Claim 10: Van Steenbrugge discloses the audio processing circuit of claim 6 but does not disclose wherein a decoding circuit and the stream recovering circuit are integrated into an audio processor of the audio processing circuit. Matsuura discloses a method for converting a data stream of a first format possibly containing an error in to a correct data stream of a second format. Matsuura shows a TS separator that decodes or parses the mpeg stream similar to block 90 of Van Steenbrugge and Matsuura further discloses an error detecting and correcting unit that repackages the signal similar to block 32 Van Steenbrugge. Matsuura further shows both of separator and the error detecting and correcting unit being integrated into an audio processor (Figure 5 of Matsuura and Figure 10 of Van Steenbrugge). It would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the blocks 90 and 98 of Van Steenbrugge since having the decoder and error detecting and correcting integrated into an audio processor as disclosed by Matsuura eliminates the possibility of an error being passed on to a unit, similar to block 90, responsible for repackaging the stream into a second format and as a result a more accurate stream is obtained (Matsuura, Paragraphs 131 and 132).

Claim 15: Van Steenbrugge discloses the method of claim 11 but *does not disclose* wherein the modifying step further comprises omitting at least one redundant bit if any redundant bit exists in the frames of the first stream. Matsuura discloses a method for converting a data stream of a first format possibly containing an error in to a correct

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data stream of a second format. Matsuura further discloses truncating or omitting redundant or extra bits in a frame when a synchronization error has occurred (Paragraph 94). It would have been obvious to one of ordinary skill in the art at the time of the invention to eliminate bits from a frame upon detecting an error as disclosed by Matsuura in the system disclosed by Van Steenbrugge since doing so allows for the second data stream formed from a corrected first data stream to be more accurate than if the first stream was not corrected (Matsuura, Paragraph 131).

Claim 19: Van Steenbrugge discloses the method of claim 11 but *does not disclose* wherein the modifying step further comprises abandoning at least one improper bit which is not capable of being modified to conform with the first standard if any improper bit exists in the frames of the first stream. Matsuura discloses a method for converting a data stream of a first format possibly containing an error into a correct data stream of a second format. Matsuura further discloses truncating or omitting redundant or extra bits in a frame when a synchronization error has occurred (Paragraph 94). It would have been obvious to one of ordinary skill in the art at the time of the invention to eliminate bits from a frame upon detecting an error as disclosed by Matsuura in the system disclosed by Van Steenbrugge since doing so allows for the second data stream formed from a corrected first data stream to be more accurate than if the first stream was not corrected (Matsuura, Paragraph 131).

Claim 20: Van Steenbrugge discloses the method of claim 11 but *does not disclose* wherein the modifying step further comprises modifying errors in the fields of the frames of the first stream. Matsuura discloses a method for converting a data stream of a first format possibly containing an error in to a correct data stream of a second format. Matsuura further discloses truncating or omitting redundant or extra bits in a frame when a synchronization error has occurred (Paragraph 94). It would have been obvious to one of ordinary skill in the art at the time of the invention to eliminate bits from a frame upon detecting an error as disclosed by Matsuura in the system disclosed by Van Steenbrugge since doing so allows for the second data stream formed from a corrected first data stream to be more accurate than if the first stream was not corrected (Matsuura, Paragraph 131).

10. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Steenbrugge in view of Asano et al. (US 2006/0026444 A1), hereinafter Asano.

Claim 17 and 18: Van Steenbrugge discloses the method of claim 16 but *does not disclose* wherein the changed field is a copyright field or an audio mode field. Asano also discloses an MPEG stream and discloses a method of copyright protection in which SCMS information is used to determine if an MPEG stream audio mode is "Copy Free" "One Generation Copy Allowed" or "Copy Prohibited" Asano does not disclose how to change the copy control bits. Since Van Steenbrugge discloses changing the content of

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a field in an MPEG stream, it would have been obvious to one of ordinary skill in the art to use the sync information provided in the MPEG stream to identify the two bit responsible for the copy control information and use the technique disclosed by Van Steenbrugge to change the bits from a "One Generation Copy Allowed" to a "Copy Prohibited" state after the disk has been read once (Asano, Paragraph 184 and 185 and Figure 5).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Saunders whose telephone number is (571) 270-1063. The examiner can normally be reached on Monday - Thursday, 9:00 a.m. - 4:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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SUPERVISORY PATENT EXAMINER